Isolation in Three-Dimensional Integrated Circuits

Alexandros Margomenos, *Student Member, IEEE*, Katherine Juliet Herrick, *Member, IEEE*, Martin I. Herman, *Senior Member, IEEE*, Sam Valas, *Associate Member, IEEE*, and Linda P. B. Katehi, *Fellow, IEEE*

***Abstract*—The necessity for high-density integrated-circuit (IC) design makes the issue of circuit isolation a critical one. In multilayer structures, surface waves excited by planar discontinuities induce parasitic currents on adjoining interconnects, therefore, causing a parasitic coupling, which becomes a limiting factor as density increases and size reduces. This paper presents a study of those proximity effects on interconnect geometry for X- and W-bands. Various configurations of finite ground microstrip lines, finite ground coplanar (FGC) waveguides, and transitions have been analyzed for silicon and Duroid substrates. The results included in this paper illustrate the implications of parasitic coupling associated with interconnects printed in parallel or perpendicular configurations, lines located in close proximity to open-end discontinuities, vias etched near FGC lines, and finally vertical transitions through wafers. Theoretical and experimental results, in terms of reduced isolation, are provided, showing the advantages of the use of FGC lines over conventional microstrip lines since, in the cases investigated, they offer 8 dB higher isolation. Additionally, open-end effects are demonstrated to increase coupling by as much as 6 dB, while vertical transitions through wafers cause a parasitic coupling in the order of 3 dB. The results presented in this study can be employed in order to reduce parasitic interference between interconnects.**

***Index Terms*—Finite ground coplanar (FGC) waveguide, isolation, micromachining, packaging.**

I. Introduction

With ever-increasing demands to produce high-density microwave modules, achieving adequate isolation between circuit elements becomes more difficult. This is a particular concern for transceiver applications where high isolation is necessary to ensure receiver sensitivity and prevent leakage between channels. Multilayer architectures incorporating complex circuits in a common substrate material pose the most challenging isolation problem. When circuits are printed on a common substrate, surface waves excited by planar discontinuities or leaky modes tend to induce parasitic currents on neighboring interconnects and circuits leading to unwanted interference. This parasitic coupling becomes increasingly more problematic as circuits are printed on multilayered structures for higher density and smaller size. In such structures, proximity effects are dependent on interconnect geometry. Appropriate layout design and relative placement of lines, vias, and vertical transitions is necessary in order to reduce any unwanted interference. It is the purpose of this paper to identify the limits imposed in isolation by three-dimensional integration and on-wafer packaging utilizing silicon micromachining.

As microstrip was the prevalent transmission line in the early 1980s, investigation of microstrip-to-microstrip crosstalk and electromagnetic coupling became a critical issue for design and simulation of monolithic microwave integrated circuits (MMICs) [1]. The inaccuracies between the theoretical results and measured data observed initiated an extensive study of crosstalk using various analytical tools and employing both quasi-static approximations and full-wave solvers. Spectral-domain methods were used in [2]–[4] where the surface waves are related with the presence of poles in the spectral Green's function associated with the problem. The parasitic crosstalk between various line configurations has also been addressed using the method of moments [5], along with the finite-element method [6] and finite-difference time-domain method [7]. In addition, for the same problem, potential and induced electromotive force (EMF) methods have been utilized in [8] and the generalized coupling model (GCM) has been used by Swanson [9]. The results of the aforementioned studies are consistent and are corroborated by the present study.

Crosstalk between adjoining interconnects is caused by a variety of mechanisms. Thus, when the distance between the lines is small compared to a dielectric wavelength, then the predominant reason for decreased isolation is near-field coupling due to open-end effects and discontinuities. However, when the separation between interconnects increases the coupling occurs due to the surface waves (TM_0 or TE_0) propagating inside the dielectric substrate. Such modes can be excited by discontinuities, but can also be launched by leaky dominant modes. Published studies [2], [3] show that a leaky dominant mode is present at higher frequencies on conventional microstrip lines printed on an isotropic substrate. This mode has a leakage into the TM_0 surface wave and exists independently of and in addition to the usual dominant mode. An important observation is that, near the strip, the leaky mode has a field distribution that closely resembles that of the bound mode. Therefore, both modes can be excited by conventional microstrip feeds. The critical frequency where the leakage onset occurs is reported to be as low as a few gigahertz depending on the substrate characteristics (thickness and dielectric constant). This leaky mode may interact with other lines or components in the microstrip package, thus accounting for an increase in crosstalk.

Manuscript received February 22, 2001; revised December 14, 2002. This work was supported by the Jet Propulsion Laboratory, Center on Integrated Space Microsystems under National Aeronautics and Space Administration Prime Contract NAS7-1407, Task Order 15139.

A. Margomenos is with the Department of Electrical Engineering and Computer Science, The University of Michigan at Ann Arbor, Ann Arbor, MI 48109-2122 USA (e-mail: amargome@engin.umich.edu).

K. J. Herrick is with the Microwave Device Research Laboratory, Raytheon RF Components, Andover, MA 01810 USA.

M. I. Herman and S. Valas are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA.

L. P. B. Katehi is with the School of Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: katehi@purdue.edu).

Digital Object Identifier 10.1109/TMTT.2002.806942

The coplanar waveguide (CPW), proposed by Wen in 1969, consists of two slots printed on a dielectric substrate. As shown in [10], the loss and dispersion of the CPW are comparable and, in some cases, better than the ones exhibited by the microstrip lines. For an infinite ground plane, the lowest order surface wave mode is the TM_0 and, at the frequency where the phase velocity of the surface wave becomes equal or smaller than the velocity of the CPW mode, highly dispersion behavior is observed. For conventional substrate thickness between 100 –500 μm, this frequency is of the order of hundreds of gigahertz. However, this is true only for infinite architectures (substrate and interconnects) and straight lines, without any discontinuities. In a realistic structure, multiple lines of finite length are printed on a common substrate of finite dimensions [11]. Additionally, these structures are usually packaged including backside metallization, top, and/or side metallic walls. The finite dimension of the interconnects, along with the packaging effects, can change the leakage properties of the lines significantly and can cause leakage to occur at much lower frequencies than expected [12], [13].

The finite ground coplanar (FGC) waveguide has an additional major advantage in its ability to suppress parasitic modes. If symmetry around the center conductor is maintained or air bridges are used to equalize the potential on the two ground planes, the coupled slot-line mode is eliminated. Reducing the total width of the line below $\lambda_g/2$ can move the cutoff frequency out of the band of operation, thus suppressing all higher order modes. Moreover, the finite-ground CPW has lower leakage constant compared with the infinite CPW [4]. In the case of the FGC line, the lowest surface wave mode is the TE_0 and, therefore, leakage occurs at higher frequencies compared to the infinite ground plane CPW line. Tsuji *et al.* in [4] also illustrates that the reduction of the ground-plane width can significantly reduce the leakage constant. A similar observation is made in [14] where the reduction of the ground-plane width increased the isolation between two FGC lines. This similarity reveals the strong relationship among the leaky modes and the crosstalk between lines.

According to previous results, the onset of leaky modes occurs at much higher frequencies for the FGC line compared with the microstrip line and, therefore, FGC lines provide a wider single-mode frequency range of operation [3], [4]. Moreover, the FGC line has less field overlap with the surface-wave modes than microstrip, and interacts weakly with them [15]. Since theoretical and experimental results indicate that the FGC line will demonstrate better isolation as compared to a microstrip line, this study focuses on FGC lines and their behavior.

Details of this study are presented below. The design and fabrication process for the X- and W-band structures is described first, followed by the results for single-layer and multilayer architectures. The paper proceeds with the investigation of open-end effects, along with the deterioration in isolation caused by the existence of vias in close proximity to interconnects. Finally, it has been shown [16] that vertical transitions may launch parasitic fields, which couple to adjoining lines and result in increased coupling, if designed improperly. The understanding of these effects on coupling and the required separation to achieve desired isolation is investigated in this research. Some initial results of this study have been presented in [17]. These include only X-band circuits and especially the FGC-to-microstrip coupling and the FGC-to FGC vertical transition. The additional X- and W-band results are novel and comprise a more complete study of the parasitic coupling at both frequency bands.

II. Design of Isolation Architectures

In view of the above, this study addresses coupling in multilayer circuits with microstrip or CPW as the underlying interconnect. The circuits under study are designed for X-band (8–12 GHz) as well as W-band (75–110 GHz) and, thus, different substrates are used. The X-band circuits are fabricated on 1.524-mm-thick Duroid with dielectric constant (ϵ) of 2.92. The W-band circuits are fabricated on high-resistivity 100-μm-thick silicon with dielectric constant of 11.7. High-resistivity silicon wafers with resistivity of 2500 $\Omega \cdot$ cm, measured by a four-point probe, are used in order to reduce the losses. Due to the high design frequency of 94 GHz, the losses are a major factor in the performance of the circuits. A static two-dimensional (2-D) electromagnetic solver is used to design a 50-Ω line for each substrate and line type (Duroid or silicon, microstrip or FGC).[1] All FGC X-band transmission lines are of dimension 1520–380–2540 μm (center conductor–aperture–ground), while all microstrip X-band transmission lines presented are of dimension 2540–7620 μm (signal conductor–ground plane). In W-band, only FGC lines are examined of dimensions 40–24–106 μm (center conductor–aperture–ground).

An efficient tool for analyzing coupling structures should allow analysis of three-dimensional topologies with vertical transitions [1] and it should account for frequency-dependent effects such as dispersion, radiation, and higher order mode propagation. All the simulation results presented in this study are obtained with HFSS, which has all of the above characteristics.[2] The structures were analyzed including conductor and dielectric losses and were surrounded by a radiation boundary, which absorbs all the incident fields simulating a free-space environment. However, the fabricated circuits always have finite dimensions and some reflections are bound to happen at the edges of the wafer due to the air–dielectric interface. These reflected fields can couple back to the lines giving slightly different measured data. Nevertheless, the simulation results acquired with this type of modeling gave results that very closely approximate the measurements in the majority of the cases.

III. Fabrication

A. X-Band Designs

The X-band circuits were fabricated on Rogers Duroid ($\epsilon = 2.94$, thickness: 1.524 mm) with the use of a milling machine. The interconnects were milled on separate wafers, which were then bonded together in order to create the multilayered structures. Cavities and vias for the vertical transitions have been

[1] *Maxwell 2-D*, ver. 3.0.25, Ansoft Corporation, Pittsburgh, PA, 2001.

[2] *High-Frequency Structure Simulator (HFSS)*, ver. 8.0, Ansoft Corporation, Pittsburgh, PA, 2001.

drilled in the dielectric substrate using appropriate milling tools. SMA connectors were soldered at the one end of each line, leaving the other open. This creates a standing wave, which, as will be shown shortly, increases the coupling by 6 dB if compared to a matched line.

B. W-Band Designs

The W-band circuits are printed on 100-μm-thick high-resistivity double-side polished silicon wafers with 6600-Å SiO_2 on both sides. Three wafers are used for the packaged isolation study and are fabricated separately. The four main fabrication steps are thin-film resistor deposition, circuit metallization, aperture definition, and anisotropic wet etching of the protective air cavities and probe windows.

For the thin-film resistors used on one of three wafers, 700 Å of TaN is deposited using a liftoff process. This thickness results in a sheet resistance of 43 Ω/square based on a four-point probe measurement. A liftoff process is also used for the circuit metallization of Cr/Au (500/9500 Å), and silicon dioxide is patterned to define cavities and probe windows. The silicon dioxide is etched partially or fully in buffered hydrofluoric acid (BHF) at the rate of 1000 Å/min. The final step is to anisotropically etch the oxide-patterned cavities and probe windows in potassium hydroxide (KOH) at an etch rate of 30 μm/h. Multiple probe windows are opened during the anisotropic etching through both wafers. Glass fibers are inserted through the windows in order to align the samples. The process is performed using an optical microscope and the expected error is of the order of 5 μm. The wafers are then bonded together using silver epoxy, which was deposited in small quantities at the wafer edges and cured at 150 °C. Since the epoxy bumps were on the edges of the wafers, far from any measured circuit, they could not affect the measured coupling.

IV. Theoretical and Experimental Results

Two different types of measurement setups are used in order to measure the various designs. For the X-band measurements SMA connectors are soldered to the interconnects and then connected to an HP 8722D vector network analyzer via 3.5-mm coaxial cables. short-open-load-through (SOLT) calibration is performed from 6 to 12 GHz using standard 3.5-mm coaxial calibration standards.

For the W-band measurements, an HP 8510C vector network analyzer is utilized on an Alessi probe station with 100-μm-pitch GGB picoprobes. Thru-reflect-line (TRL) calibration is performed using on-wafer calibration standards fabricated in conjunction with the circuits to be tested. *Multical*, developed by NIST is used to implement the TRL calibration.[3]

Prior to the measurements, all the samples are mounted on 1-mm-thick glass slides using photoresist. This was done in order to provide structural protection to the samples during the measurements and also to ensure that the coupling measured is not affected by the metallic base of the probe station. For both frequency bands, the coupling between the lines is taken as the insertion loss between the two inputs leaving the other two open, as seen in Fig. 1. A basic limitation to all the measurements presented is the undesired signal coupling, which is generated by two independent mechanisms: free-space parasitic radiation and substrate radiation. The former couples the probes when they are in noncontact position and separated by a distance equal to the distance between the two neighboring interconnects. The latter is due to surface waves that are excited in the substrate from the probes as they contact the surface of the layer. The noise floor for the X-band measurements was approximately -60 dB and for the W-band -50 dB.

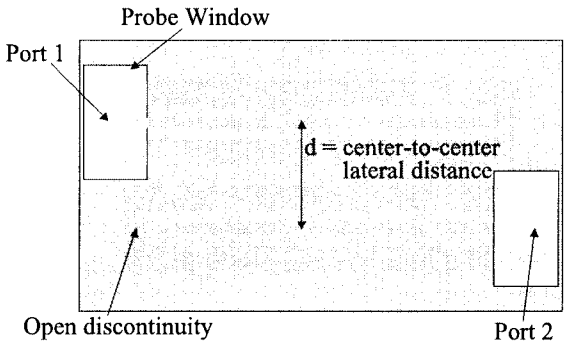


Fig. 1. Schematic for laterally separated FGC lines showing center-to-center separation and location of probe windows.

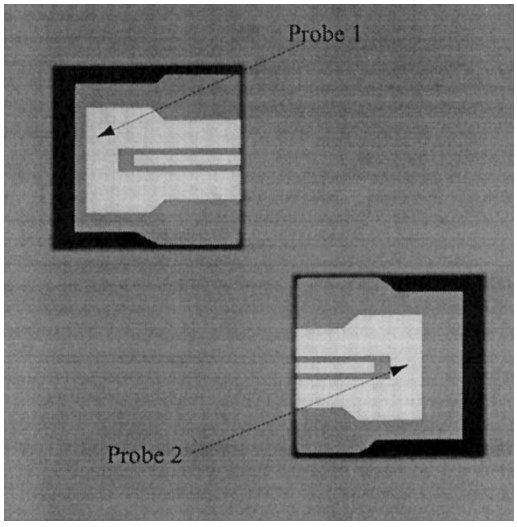
A. Single-Layer Isolation

Parallel interconnect lines patterned on the same lateral plane are a very common configuration in the majority of MMICs. Usually the lines are connecting various active or passive components and therefore they are matched reducing any undesired reflections and achieving maximum power transfer. Thus, no standing wave is generated on the line due to open-end effects. Parallel FGC lines (both open and matched) fabricated on 100-μm-high-resistivity silicon wafers are showed in Fig. 2. The distance between the center conductors is varied from 450 to 1100 μm (the dielectric wavelength at 94 GHz is 930 μm). The results for the average isolation over the respective frequency band are shown in Fig. 3 where measured and numerical results are presented. The measurements are consistent with the simulated results down to the noise floor, and illustrate the superior isolation of FGC lines of better than -45 dB for center-to-center distances larger than 800 μm. The second important observation indicated by the same graph is the fact that the open and matched FGC's differ by 6 dB, as theoretically expected, due to the existence of the standing wave in the open lines.

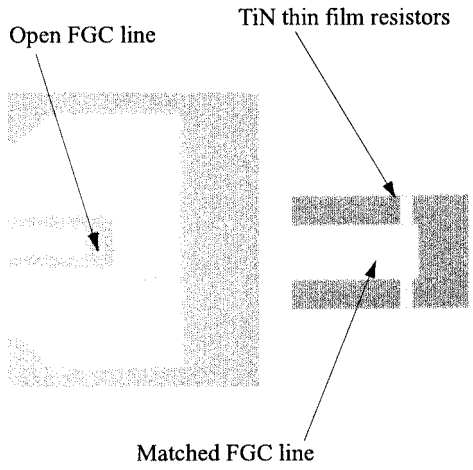
B. Multilayer Isolation

1) Parallel Architectures: A multilayer environment can include parallel lines printed in close proximity on two vertically separated planes. Both X- and W-band measurements and simulations are performed in this configuration. The fabricated X-band structure consists of a combination of a microstrip and an FGC line printed on Duroid (thickness: 1.524 mm) with a lateral separation varied from 0 to 25.4 mm. The results for the average coupling are shown in Fig. 4, where the agreement between theory and measurements degrades as the distance becomes large and the coupling is comparable to the noise floor.

[3]R. B. Marks and D. F. Williams, *Program MultiCal*, rev. 1.00, Aug. 1995.



(a)



(b)

Fig. 2. W-band circuits. (a) Packaged FGC lines printed on a 100-μm silicon wafer. (b) Detailed view of open and matched FGC line terminations.

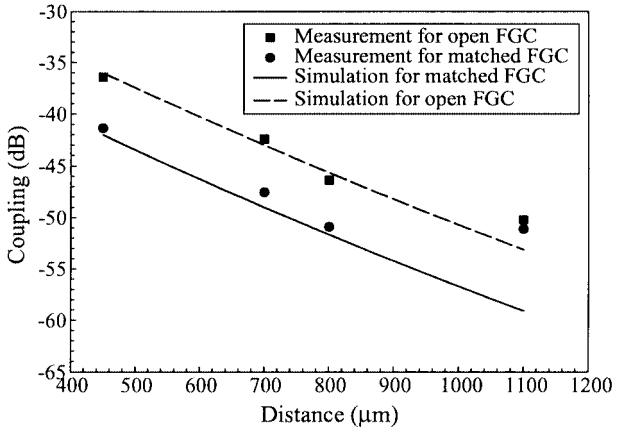


Fig. 3. W-band measured and numerical results for laterally separated FGC lines showing coupling versus center-to-center spacing.

Note that, when the two lines are exactly on top of each other, the isolation between them is -15 dB, but when the distance approaches one wavelength (21 mm), the coupling reduces to -60 dB. Simulated results for microstrip-to-microstrip and FGC-to-FGC lines are included on the same graph. In agreement with the theory presented in [4], the FGC offers better isolation compared to the microstrip by a factor of 8 dB. However, the combination of microstrip and FGC line offers an isolation that is comparable to the FGC–FGC structure for distances up to 12 mm. These two different types of lines propagate modes, which are orthogonal to each other, hence, when they are printed in close proximity, their fields couple very weakly. When the distance between the lines is expanded, the fields leak to the lower substrate mode, which, thus, becomes the main mechanism that causes increased crosstalk. Therefore, the use of the microstrip–FGC combination could be an alternative design if the use of microstrip lines in a specific circuit is unavoidable.

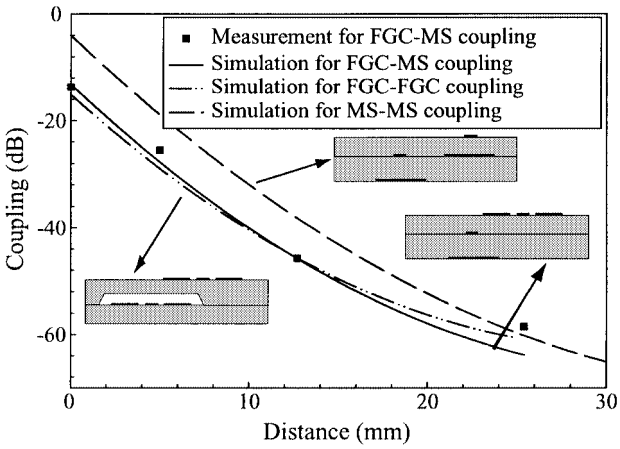


Fig. 4. X-band measured and numerical results for vertically separated FGC and microstrip lines showing coupling versus center-to-center spacing.

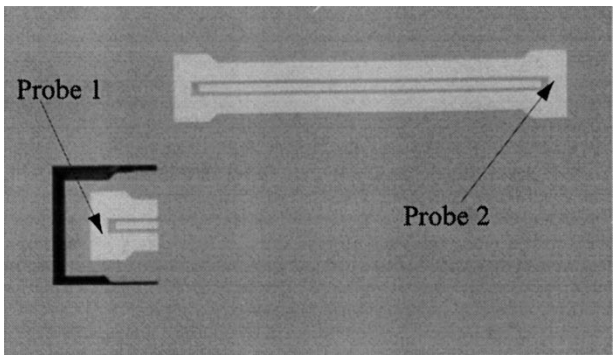


Fig. 5. W-band FGC lines printed on two 100-μm silicon wafers.

Parallel W-band FGC lines were fabricated on two 100-μm-high-resistivity silicon wafers, which were bonded together using silver epoxy. The center-to-center distance varied from 0 to 1100 μm and the circuits are shown in Fig. 5. Measured and simulation results for average coupling over the respective frequency band are shown in Fig. 6, where, again, there is a consistency between simulation and measurements. When the lines are exactly on top of each other, the isolation between them is -19 dB; when the distance approaches one wavelength (930 μm), the isolation increases to -49 dB. In the initial configuration, when the two FGC lines are perfectly aligned and the center-to-center distance is zero, the measured response displays a 10-dB ripple over the frequency of interest. This is attributed to a parallel-plate mode that is excited due to the close

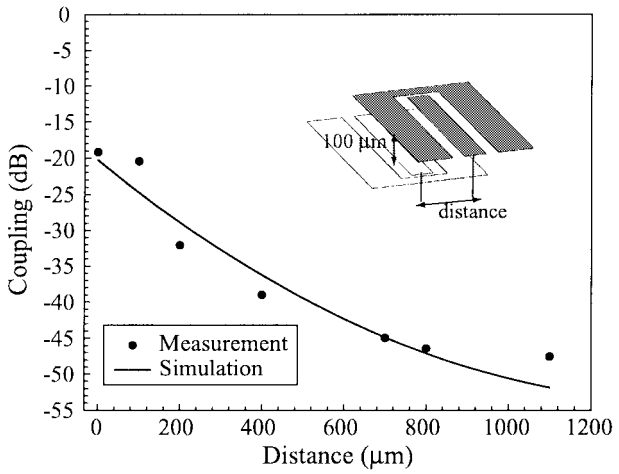


Fig. 6. W-band measured and numerical results for vertically separated FGC lines showing coupling versus center-to-center spacing.

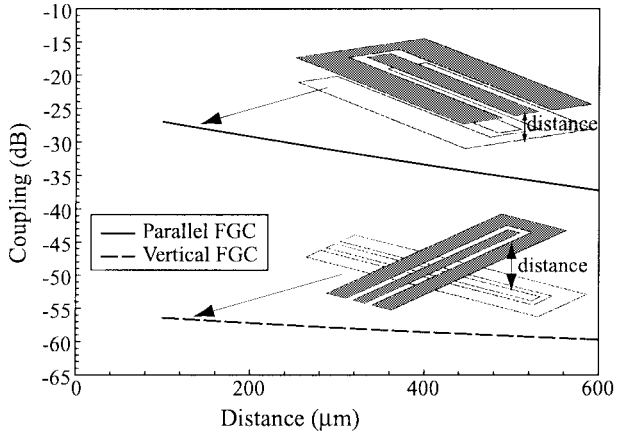


Fig. 7. Numerical results for vertically separated parallel and perpendicular FGC lines comparing coupling versus vertical separation at 8 GHz.

proximity of the two ground planes. This ripple is significantly reduced as the lines are separated resulting in a 5-dB ripple at 400-μm distance and a 2-dB ripple at 800 μm. The results summarized in Fig. 6 correspond to the ripple peak. This ripple is expected to be lower if the two lines are matched, however, such a placement of two parallel FGC lines should be avoided if high isolation is needed.

2) Perpendicular Architectures: In order to investigate the effects of the vertical separation to various FGC lines configurations, multiple simulations for X-band structures are performed. The lines are design to be 50 Ω (106–24–40 μm) printed on 100-μm silicon wafers. A set of parallel and a set of perpendicular FGC lines are analyzed at 8 GHz and the results are displayed in Fig. 7 along with the schematics of the two structures, where the dielectric and cavities have been omitted for illustration purposes. As expected, the perpendicular lines offer much better isolation (always better than -55 dB) since the interaction of the two lines is restricted to the crossover area. This is not the case in the parallel FGC lines, where the coupling is -26 dB for 100 μm of vertical distance and is decreased to -35 dB at 500 μm. Therefore, when designing for high isolation in multilayered structures, perpendicular FGC lines should be considered.

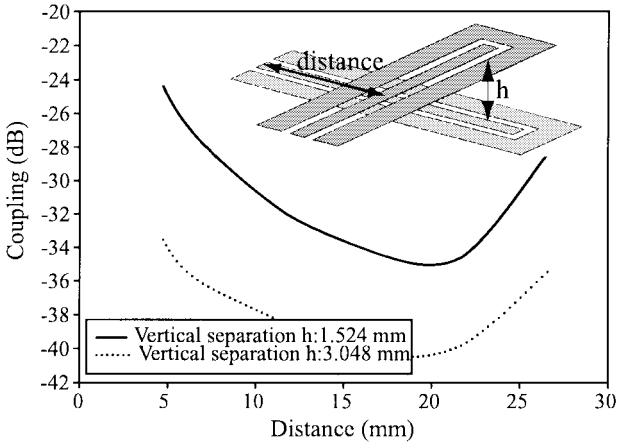


Fig. 8. Numerical results for vertically separated perpendicular FGC lines showing coupling versus distance at 8 GHz.

Additionally, perpendicular FGC lines are studied in terms of their lateral separation. Two 50-Ω lines (2540–381–1524 μm) are printed perpendicularly in Rogers Duroid ($\epsilon = 2.94$, thickness: 1524 μm), the vertical distance between them is one and two wafer thicknesses (1524 and 3048 μm), respectively. Both lines are centered with respect to each other and the top line is moved laterally with respect to the lower one. The simulation results are displayed in Fig. 8 along with a schematic of the structure. From the results, it is apparent that the isolation increases as the top FGC line moves away from the probing position. This trend continues until the top FGC line approaches the open end of the lower line. As expected, the discontinuity effects increase the coupling significantly. These results display the importance of probe placement for accurate coupling estimation. If the separation between the probes is small, the dominant effect responsible for reducing isolation will be the probe-to-probe coupling. On the other hand, if the lines are printed close to discontinuities, less isolation should be expected. The lines in Fig. 8 are identical with the X-band results summarized in Fig. 4. The comparison between the plots indicates that the perpendicular FGC lines with a vertical separation of 1.524 mm offer an isolation of -31.6 dB, while the parallel FGC couple at -14 dB.

A similar structure for W-band measurements is fabricated in high resistivity 100-μm silicon wafers. The fabricated circuits are shown in Fig. 9 and the results are presented in Fig. 10, where an isolation better than -42 dB is measured. As the two lines are separated, the isolation increases to -47 dB for a distance of 500 μm. These results compared to those provided in Fig. 8 show a similar behavior of the perpendicular lines with respect to the lateral separation. A small offset of the two lines can improve the isolation by 3–4 dB. However, as was mentioned earlier, increased coupling should be expected if the open end is in close proximity with the top FGC line.

Another important factor when designing multichip modules is the use of vias for vertical transmission of signals or dc-bias lines to multiple stacked wafers. The effects of one via in close proximity of two perpendicular FGC lines with a vertical separation of 100 μm are presented in Fig. 11 along with a schematic of the structure. The via is designed as a rectangular box with

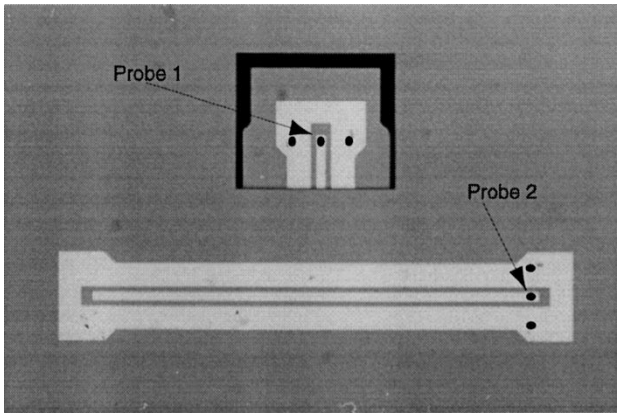


Fig. 9. W-band perpendicular FGC lines printed on two 100-μm silicon wafers.

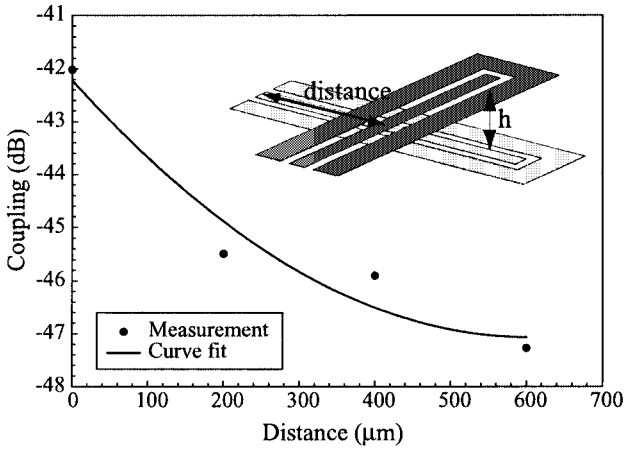


Fig. 10. W-band measured results for vertically separated FGC lines showing coupling versus distance.

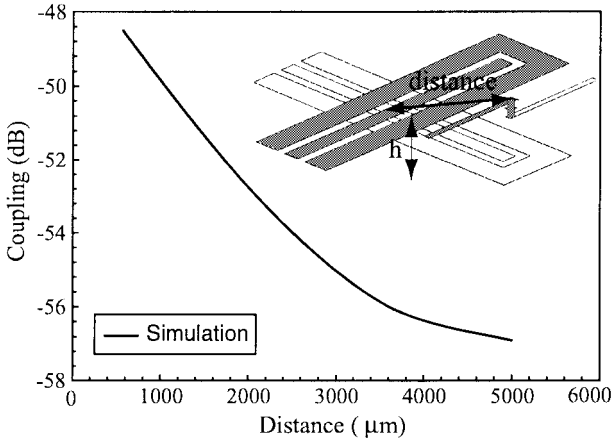


Fig. 11. X-band numerical results for vertically separated FGC lines adjacent to via showing coupling versus via to cross-sectional distance.

80-μm width and it is terminated on both ends with a $\lambda_g/4$ resonant stub. Such a configuration is viewed as a worst case scenario and its purpose is to demonstrate the effects on crosstalk of a parasitic element with a strong standing wave due to the open stubs. The lines are identical to the interconnects analyzed in Fig. 7 and, therefore, completely comparable with the data summarized in that plot. The existence of the via deteriorates the

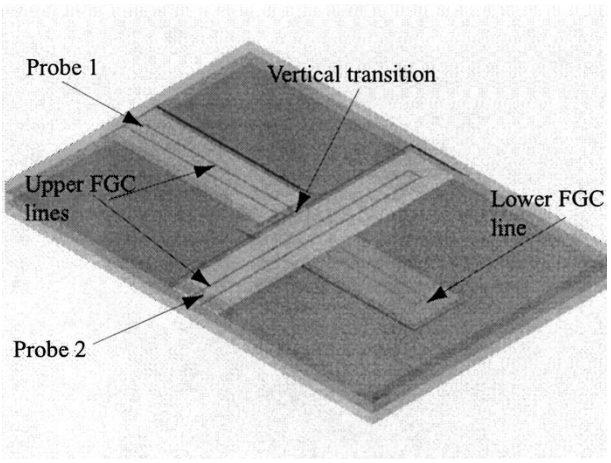


Fig. 12. Schematic for X-band FGC-to-FGC vertical transition.

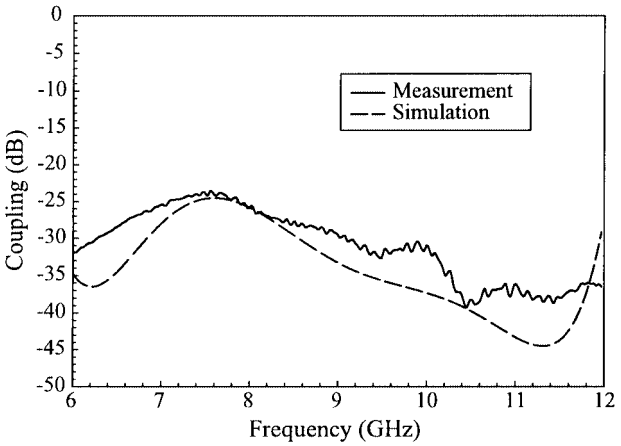


Fig. 13. X-band measured and numerical results for vertically separated FGC lines incorporating via transition.

isolation as much as 9 dB, when the via is in close proximity to the crossover section of the two lines. When the distance is increased over 2000 μm, the coupling approximates the ideal case (no via present). The need of vias in a multilayered structure is inevitable; therefore, their appropriate placement is an important design consideration, significantly affecting the isolation.

Moreover, vias are utilized in multilayered interconnects as a conducting path for vertical transition in different wafers. Fig. 12 shows the schematic of the fabricated X-band circuit consisting of an FGC transitioned through a wafer and printed in close proximity (2794 μm) to a second FGC line. The transition is accomplished using vias with a diameter of 1200 μm. In order to reduce coupling, dielectric cavities with a height of 762 μm are milled on top of all three lines. The isolation with respect to the frequency is shown in Fig. 13 where both measurements and simulation results are included. The measurements reveal a 10-dB variation in the coupling between the two lines. This ripple is due to the length of the interconnects utilized in this transition and not a result of an undesired tuning effect since all the FGC lines are 50-Ω matched interconnects and the dielectric cavities surrounding them resonate well above the investigated frequency band. An isolation of -25 dB at 8 GHz is observed. In order to investigate the improvement

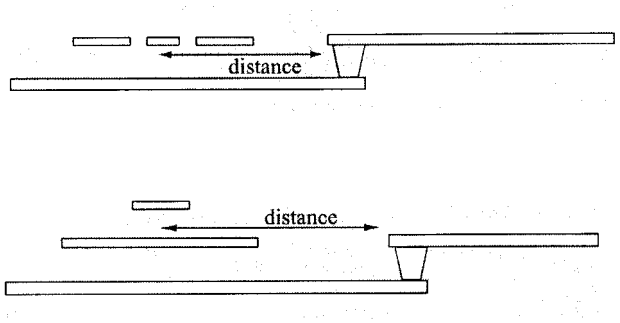


Fig. 14. Schematics for X-band vertical transitions.

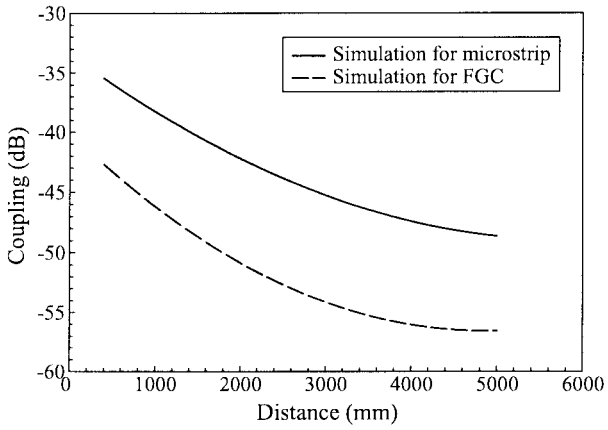


Fig. 15. Numerical results for vertically separated FGC and microstrip lines incorporating via transition showing coupling versus distance at 8 GHz.

in the performance caused by the cavities, another structure was simulated where the dielectric cavity of the top FGC line, which is printed in close proximity with the vertical transition, was inverted. The creation of an extra air layer between the two FGCs increased the isolation to -30 dB at 8 GHz. The simulation of the same perpendicular FGCs, without the vertical transition, shows an isolation of -28 dB for the same frequency. These simulations were conducted over the whole X-band frequency range in order to verify that the changes in isolation noticed were not a result of a small frequency perturbation. Consequently, the vertical transition lowered the isolation by 3 dB, while the different placement of the cavities increased the isolation by 5 dB.

As was already mentioned, the vertical transition launches a parasitic mode, which couples to the neighboring lines. X-band simulations were performed in order to investigate the variations of this coupling with respect to the distance. The two structures analyzed are presented in Fig. 14 where the parameter under consideration is the distance between the edge of the vertical transition and the edge of the line. Two sets of simulations were done for a top line being either a microstrip or an FGC line. Both lines were designed to be 50 Ω (FGC: 106–24–40 μm, microstrip: 45–400 μm) in silicon. As seen in Fig. 15, both structures have a similar response with respect to the distance from the vertical transition, exhibiting an increase of 13 dB in isolation as the distance changes from 400 to 5000 μm. The FGC line shows less coupling compared to the microstrip line by a factor of 8 dB. In the case of the microstrip line, the existence of the ground plane reduces the coupling between the line and lower FGC. This fact means that the parasitic field launched at the top edge of the vertical transition is probably the main reason for the increased coupling between the lines. Therefore, as was reported above, careful design and appropriate placement of cavities is necessary in order to ensure high isolation.

V. Conclusions

A study of W- and X-band circuits has been presented, providing results that can be utilized for the design and fabrication of high-isolation systems. FGC lines in comparison to microstrip have been shown both theoretically and experimentally to give 8 dB higher isolation for the specific cases and frequency ranges investigated. Interconnects printed in a single or multiple layers and separated by a distance equal to one dielectric wavelength demonstrate an isolation of -50 or -60 dB for W- and X-band, respectively. Moreover, lines printed in close proximity to open-end discontinuities suffer a degradation in parasitic coupling of as much as 6 dB. Furthermore, the micromachining of dielectric cavities has been studied and shown to provide an increase in isolation of the order of 5 dB. The existence of vias next to RF interconnects has been investigated as a worst case scenario and has demonstrated reduced isolation by 9 dB. Finally, the launching of parasitic modes from vertical transitions has been studied both analytically and experimentally, showing the importance of appropriate placement of cavities in order to ensure high isolation.

References

[1] M. Goldfarb and A. Platzker, "The effects of electromagnetic coupling on MMIC design," *Int. J. Microwave Millimeter Wave Computer-Aided Eng.*, vol. 1, no. 1, pp. 38–47, June 1991.

[2] A. A. Oliner and K. S. Lee, "The nature of the leakage from higher modes on microstrip line," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Baltimore, MD, June 1986, pp. 57–60.

[3] D. Nghiem, J. T. Williams, D. R. Jackson, and A. A. Oliner, "Existence of a leaky dominant mode on microstrip line with an isotropic substrate: Theory and measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 1710–1715, Oct. 1996.

[4] M. Tsuji, H. Shigesawa, and A. A. Oliner, "New interesting leakage behavior on coplanar waveguides of finite and infinite widths," *IEEE Trans. Microwave Theory Tech.*, vol. 39, pp. 2130–2137, Dec. 1991.

[5] C. Wei, R. F. Harrington, J. R. Mautz, and T. K. Sarkar, "Multi-conductor transmission lines in multilayered dielectric media," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 439–450, Apr. 1984.

[6] C. E. Free, K. P. Tang, D. Li, K. E. G. Pitt, and P. Barnwell, "High frequency interconnections and crosstalk on MCM structures," in *Int. Microelectron. Symp.*, Minneapolis, MN, Oct. 1996, pp. 522–525.

[7] P. S. Bhattachargee, S. Das, and S. K. Chowdhury, "Coupling between microstrip transmission lines," in *Int. Electromagn. Interference and Compat. Conf.*, Madras, India, Dec. 1995, pp. 78–81.

[8] D. A. Hill, K. H. Cavcey, and R. T. Johnk, "Crosstalk between microstrip transmission lines," *IEEE Trans. Electromagn. Compat.*, vol. 36, pp. 314–321, Nov. 1994.

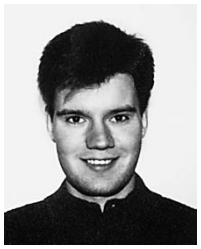
[9] D. G. Swanson, "A novel method for modeling coupling between several microstrip lines in MIC's and MMIC's," *IEEE Trans. Microwave Theory Tech.*, vol. 93, pp. 919–923, June 1991.

[10] R. W. Jackson, "Considerations in the use of coplanar waveguide for millimeter-wave integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-34, pp. 1450–1456, Dec. 1986.

[11] L. Carin, G. W. Slade, and K. J. Webb, "Mode coupling and leakage effects in finite-size printed interconnects," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 450–457, May 1998.

[12] A. A. Oliner, "Package effects caused by leaky modes at higher frequencies in microwave integrated circuits," in *Eur. Microwave Conf. Dig.*, Munich, Germany, Sept. 1999, pp. 122–125.

[13] F. Mesa, A. A. Oliner, D. R. Jackson, and M. J. Freire, "The influence of a top cover on the leakage from microstrip line," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 2240–2248, Dec. 2000.
[14] G. E. Ponchak, E. M. Tentzeris, and L. P. B. Katehi, "Characterization of the coupling between adjacent finite ground coplanar (FGC) waveguides," *Int. J. Microcircuits Electron. Packag.*, vol. 20, no. 4, pp. 587–592, Nov. 1997.
[15] M. Riaziat, R. Majidi-Ahy, and I. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 245–250, Mar. 1990.
[16] K. J. Herrick, J. G. Yook, and L. P. B. Katehi, "Microtechnology in the development of three-dimensional circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1832–1844, Nov. 1998.
[17] A. Margomenos, S. Valas, M. I. Herman, and L. P. B. Katehi, "Isolation in three-dimensional integrated circuits," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, June 2000, pp. 1875–1878.



Alexandros Margomenos (S'99) was born in Thessaloniki, Greece, in 1975. He received the B.Sc. degree in physics from the Aristotle University of Thessaloniki, Thessaloniki, Greece, in 1998, the M.Sc. degree in electrical engineering and computer science from The University of Michigan at Ann Arbor, in 2000, and is currently working toward the Ph.D. degree at The University of Michigan at Ann Arbor.

His research interests include microwave and millimeter-wave circuits, silicon micromachining, three-dimensional integration, and packaging. He is currently involved with the design and implementation of packages for RF microelectromechanical system (MEMS) switches. He has a patent pending in the area of packaging of RF MEMS.

Katherine Juliet Herrick (S'91–M'00) received the B.S.E, M.S.E., and Ph.D. degrees in electrical engineering from The University of Michigan at Ann Arbor, in 1994, 1996, and 2000, respectively. Her doctoral dissertation concerned integrated three-dimensional microwave circuits up to W-band utilizing silicon micromachining.

She is currently a Senior Research Scientist with the Microwave Device Research Laboratory, Raytheon RF Components, Andover, MA, where she is involved with high-frequency metamorphic high electron-mobility transistor (MHEMT) technologies, microwave circuit design, and integrated arrays through 110 GHz. Prior to joining Raytheon in January 2001, she conducted research as a Post-Doctoral Research Fellow in the areas of packaged MEMS and multilayer silicon circuits. She holds one patent.

Dr. Herrick was the recipient of the 1997 and 2000 Best Student Paper Award presented at the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS).

Martin I. Herman (S'78–M'87–SM'92) received the B.S.E.E. degree from Drexel University, Philadelphia, PA, in 1982, and the M.S.E.E. and Ph.D. degrees from The University of Michigan at Ann Arbor, in 1983, and 1987, respectively.

From 1987 to 1992, he was with GM–Hughes, where he was responsible for GaAs microwave and millimeter-wave circuit development and characterization. In 1992, he joined Jet Propulsion Laboratory (JPL), California Institute of Technology, Pasadena, where he is currently Deputy Manager of The Microwave Experiment Systems and Technology Section. During his past ten years with the JPL, he was the leader of the Deep Space One Telecommunication Subsystem (1995–1998), which successfully developed and demonstrated advanced deep space Ka-band communication technology in space. He was the leader for the Advanced RF Front-End System-On-A-Chip Task for JPL's Center for Integrated Space Microsystems (CISM), as well as for other advanced telecommunication research and development tasks. His research interests include electromagnetic scattering, high-frequency packaging technology, antennas, monolithic integrated microwave/millimeter-wave circuits, high-frequency measurement techniques, communication systems, and advanced solid-state device technology. He holds one U.S. patent in the area of automotive radar technology.

Dr. Herman was the Los Angeles chair for the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) for 1990 and 1991. He was a Distinguished National Lecturer for the IEEE Antenna and Propagation Society (IEEE AP-S) (1996–1997). He is a member of Eta Kappa Nu, Phi Kappa Phi, Sigma Xi, Tau Beta Pi, and the American Institute of Aeronautics and Astronautics (AIAA). He was the recipient of a Howard Hughes Doctoral Fellowship. He was also the recipient of the JPL Award for Exceptional Technical Excellence, six National Aeronautics and Space Administration (NASA) Technical Brief Awards, the NASA Group Achievement Award, the JPL Director's Discretionary Fund Award, and the California Institute of Technology President's Discretionary Fund.

Sam Valas (A'93) received the B.S. degree in electrical engineering from the University of California at Los Angeles, in 1986, and the M.S. degree in electrical engineering from the University of Southern California, Los Angeles, in 1991.

From 1987 to 1992, he was with the Hughes Aircraft Company, where he designed and developed microwave components and subassemblies including low-noise amplifiers (LNAs), power amplifiers, transceivers, and advanced MMICs. In 1992, he joined the Jet Propulsion Laboratory (JPL), California Institute of Technology, Pasadena, where he was initially involved in the development of telecommunications hardware for deep-space missions. In 1998, he led a task to evaluate and develop MEMS technology for high-frequency radar applications. He is currently a Senior Systems Engineer, responsible for the design of telecommunications subsystems for near-earth and deep-space missions. He has a patent pending in the area of MEMS circuit design.

Mr. Valas was the recipient of the Hughes Aircraft Company Division Award for his work in MMIC design. He was also the recipient of three NASA Group Achievement Awards for contributions to the Cassini, Mars Pathfinder, and New Millennium DS1 missions.

Linda P. B. Katehi (S'81–M'84–SM'89–F'95) received the B.S.E.E. degree from the National Technical University of Athens, Athens, Greece, in 1977, and the M.S.E.E. and Ph.D. degrees from the University of California at Los Angeles, in 1981 and 1984, respectively.

In September 1984, she joined the faculty of the Electrical Engineering and Computer Science Department, The University of Michigan at Ann Arbor, as an Assistant Professor, and then became an Associate Professor in 1989 and Professor in 1994. She has served in many administrative positions, including Director of Graduate Programs, College of Engineering (1995–1996), Elected Member of the College Executive Committee (1996–1998), Associate Dean For Graduate Education (1998–1999), and Associate Dean for Academic Affairs (since September 1999). She is currently the Dean of the Schools of Engineering, Purdue University, West Lafayette, IN. She has authored or coauthored 410 papers published in refereed journals and symposia proceedings and she holds four U.S. patents. She has also generated 20 Ph.D. students.

Dr. Katehi is a member of the IEEE Antennas and Propagation Society (IEEE AP-S), the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), Sigma Xi, Hybrid Microelectronics, and URSI Commission D. She was a member of the IEEE AP-S AdCom (1992–1995). She was an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION. She was the recipient of the 1984 IEEE AP-S W. P. King (Best Paper Award for a Young Engineer), the 1985 IEEE AP-S S. A. Schelkunoff Award (Best Paper Award), the 1987 National Science Foundation Presidential Young Investigator Award, the 1987 URSI Booker Award, the 1994 Humboldt Research Award, the 1994 University of Michigan Faculty Recognition Award, the 1996 IEEE MTT-S Microwave Prize, the 1997 International Microelectronics and Packaging Society (IMAPS) Best Paper Award, and the 2000 IEEE Third Millennium Medal.